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EXAMINER	
BEHM, HARRY RAYMOND	
ART UNIT	**PAPER NUMBER**
2838	

DATE MAILED: 09/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/821,460	KHAYKIN ET AL.	
	Examiner	Art Unit	
	Harry Behm	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 April 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/9/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the P-channel MOSFET as claimed in Claim 7 must be shown or the feature(s) canceled from the claim(s). Additionally, the connection between a body of the first and second transistors must be shown, as claimed in Claim 11. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities: The specification states 'transistor 20 is shown as a P-channel MOSFET', however an N-channel MOSFET is shown in the figures. In addition, paragraph 20 of the specification reads 0.88 volts at 40 degrees C, but should read at –40 degrees C.

Appropriate correction is required.

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Precharge circuit that adjusts inrush current with temperature.

Claim Objections

Claim 8 is objected to because of the following informalities: 'configured transfer heat' should be 'configured to transfer heat'. Appropriate correction is required.

Claim 11 is objected to because 'a body' of the transistor is not defined making it unclear whether Applicant intends to claim a connection to the substrate, also known as the body, or intends a connection to the exterior of the transistor, such as a lead or the package.

Claim 18 is objected to because of the following informalities: 'the diode' and 'the cathode' lack antecedent basis, making it unclear whether 18 depends on 13 or 17. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 8-9, 11, 13-14 and 19-20 rejected under 35 U.S.C. 102(b) as being anticipated by Rampold (US 6,094,036).

With respect to Claim 1, Rampold discloses a precharge circuit (Fig. 6) comprising: a power source (Fig. 6 T1); a first transistor (Fig. 6 FET2) in electrical communication with the power source; and a second transistor (Fig. 6 T) in electrical communication with the first transistor, the second transistor configured to provide feedback (Fig. 6 gate) to the first transistor and adjust current [gate controls current] flowing through the first transistor based on a temperature of the first transistor [FET heats BJT which causes a higher resistance in the FET].

With respect to Claim 2, Rampold discloses the precharge circuit according to claim 1, wherein the second transistor (Fig. 6 T) is configured to decrease current flowing through the first transistor as the temperature of the first transistor increases [FET heats BJT which causes a higher resistance in the FET].

With respect to Claim 3, Rampold discloses the precharge circuit according to claim 2, wherein the second transistor (Fig. 6 T) is a bipolar transistor [PNP BJT].

With respect to Claim 8, Rampold discloses the precharge circuit according to claim 3, further comprising a thermal conductor (Fig. 6 gate) connecting the first and second transistor and configured to transfer heat [copper trace conducts heat] from the first transistor (Fig. 1 Q2 gets hotter at inrush) to the second transistor (Fig. 6 T).

With respect to Claim 9, Rampold discloses the precharge circuit according to claim 8, wherein the thermal conductor (Fig. 6 gate) is a circuit trace [it is understood that power supplies, inventions required to be reliable or other modern applications are implemented on a PCB with circuit traces].

With respect to Claim 11, Rampold discloses the precharge circuit according to claim 8, wherein the thermal conductor (Fig. 6 trace connecting gate to collector) is connected between a gate (Fig. 6 FET2 gate) of the first transistor and a collector (Fig. 6 T collector) of the second transistor.

With respect to Claim 13, Rampold discloses the precharge circuit according to claim 3, wherein a collector (Fig. 6 T collector) of the second transistor (Fig. 6 T) is connected to a gate of the first transistor (Fig. 6 FET2 gate).

With respect to Claim 14, Rampold discloses the precharge circuit according to claim 13, further comprising a sense resistor (Fig. 6 R) connected between the power source (Fig. 6 T2 returns to power source) and a source of the first transistor (Fig. 6 FET2 source).

With respect to Claim 19, Rampold discloses the precharge circuit according to

claim 13, wherein an emitter of the second transistor (Fig. 6 T emitter) is in electrical communication with the power source [emitter senses the voltage of the power source minus the voltage drop of the FET and the sense resistor]

With respect to Claim 20, Rampold discloses the precharge circuit according to claim 13, wherein a drain of the first transistor (Fig. 6 FET2 drain) is in electrical communication [drain connected to voltage ground plus voltage C1 plus voltage R + voltage FET drain to source) with an electrical ground (Fig. 2 T3) through a capacitor (Fig. 2 C1).

Claims 1-7, 28 rejected under 35 U.S.C. 102(e) as being anticipated by Fey (US 6,992,467).

With respect to Claim 1, Fey discloses a precharge circuit (Fig. 2) comprising: a power source (Fig. 2 Ue); a first transistor (Fig. 2 Q1) in electrical communication with the power source; and a second transistor (Fig. 2 Q2) in electrical communication with the first transistor, the second transistor configured to provide feedback (Fig. 2 Q2 3) to the first transistor and adjust current [gate controls current] flowing through the first transistor based on a temperature of the first transistor [FET heats BJT which increases the collector current which increases the gate voltage which causes a higher resistance in the FET thereby limiting and regulating the inrush current through the FET].

With respect to Claim 2, Fey discloses the precharge circuit according to claim 1, wherein the second transistor (Fig. 2 Q2) is configured to decrease current flowing through the first transistor as the temperature of the first transistor increases [FET heats BJT which causes a higher resistance in the FET].

With respect to Claim 3, Fey discloses the precharge circuit according to claim 2, wherein the second transistor (Fig. 2 Q2) is a bipolar transistor [PNP BJT].

With respect to Claim 4, Fey discloses the precharge circuit according to claim 3, wherein the second transistor (Fig. 2 Q2) is a PNP transistor. [PNP BJT]

With respect to Claim 5, Fey discloses the precharge circuit according to claim 4, wherein the second transistor (Fig. 2 Q2) has a negative base-emitter voltage temperature coefficient [inherent for PNP BJT].

With respect to Claim 6, Fey discloses the precharge circuit according to claim 5, wherein the first transistor (Fig. 2 Q1) is a MOSFET [P MOSFET].

With respect to Claim 7, Fey discloses the precharge circuit according to claim 6, wherein the first transistor (Fig. 2 Q1) is a P-channel MOSFET.

With respect to Claim 28, Fey discloses a precharge circuit (Fig. 2) comprising: a power source (Fig. 2 Ue); a P-channel MOSFET transistor (Fig. 2 Q1) in electrical communication with the power source; a bipolar PNP transistor (Fig. 2 Q2) in electrical communication with the P-channel MOSFET transistor, the bipolar PNP transistor configured to provide negative feedback [as the base emitter-votlage of Q2 increases, the collector current increases which raises the gate voltage and causes Q1 to limit the current] to the P-channel MOSFET transistor and decrease current flowing through the P-channel MOSFET transistor as the temperature of the P-channel MOSFET transistor increases [as Q1 conducts current and heats up, Q2 will conduct and be heated, which increases the conductor current]; and a thermal conductor (Fig. 2 Q2 3 trace) connected between a collector (Fig. 2 Q2 3) of the bipolar PNP transistor and a gate (Fig. 2 Q1 G)

of the P-channel MOSFET, the thermal conductor [copper trace] being configured to transfer heat from the P-channel MOSFET to the bipolar PNP transistor.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 10,15 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rampold (US 6,094,036).

With respect to Claim 10, Fey discloses the precharge circuit according to claim 9, but does not disclose the width of the circuit trace (Fig. 6 gate). It would have been obvious to one of ordinary skill in the art at the time of the invention to make the trace have a width of greater than 2 mm. The reason for doing so is critical traces are routinely made wider.

Claims 15 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fey (US 6,992,467).

With respect to Claims 15 and 30, Fey discloses the precharge circuit set forth above, using a sense resistor R1. Fey does not disclose the wattage of the sense resistor since component selection is well known. It would have been obvious to one of ordinary skill in the art at the time of the invention to select a sense resistor such that the wattage is less than 1 Watt. The reason for doing so is to reduce the power wasted through heating of the resistor.

Claims 1 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fey (US 6,992,467) in view of the MMBTA56 datasheet.

With respect to Claims 1 and 28, Fey discloses the precharge circuit as set forth above, but does not disclose the exact BJT to be used as component selection is well known in the art. The MMBTA56 datasheet teaches that the transistor has an increasing collector current with temperature and the maximum collector current should be held less than 500mA. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the MMBTA56 for Q2. The reason for doing so is "The device is designed for general purpose amplifier applications at collector currents to 300mA" (MMBTA56 datasheet, pages 1 and 3).

With respect to Claims 12 and 29, Fey discloses the precharge circuit as set forth above, wherein the second transistor (Fig. 6 T) is positioned near the first transistor (Fig. 6 FET2). Fey does not disclose how close Q1 must be placed to Q2 as PCB layout is well know in the art. Wittenberg teaches implementing the precharge circuit on an integrated circuit. It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the precharge circuit as an integrated circuit so the second transistor is within about 5 mm or closer from the first transistor. The reason for doing so is to reduce the size and cost as well as increasing the reliability of the precharge circuit.

Claims 16-18 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fey (US 6,992,467) in view of Bernstein (US 5,420,780).

With respect to Claims 16-18 and 31, Fey discloses the precharge circuit as set forth above, but does not disclose the use of a diode. Bernstein teaches the use of a diode in a precharge circuit. It would have been obvious to one of ordinary skill in the art at the time of the invention to place a diode connected between the power source and a source of the first transistor, wherein the anode of the diode is connected to the power source and the cathode of the diode is connected to the source of the first transistor and wherein a base of the second transistor is connected to the cathode of the diode through a resistor. The reason for doing so is to prevent potentially damaging reverse current flow from the output capacitors to the supply.

Claims 21-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rampold (US 6,335,654) in view of Bingsley (US 4,631,470).

With respect to Claims 21-25, Rampold discloses the precharge circuit as set forth above. Rampold does not disclose a third transistor in electrical communication with an input node, the first transistor, and the second transistor. Bingsley teaches a precharge circuit wherein the third transistor is an NPN transistor and wherein a base of the third transistor is connected to the input node through a first resistor. It would have been obvious to one of ordinary skill in the art at the time of the invention to connect an on/off switch connected to ground. The reason for doing so is to turn the device on or off.

Claims 26-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rampold (US 6,335,654) in view of Ninh (US 5,920,186).

With respect to Claims 26-27, Rampold discloses the precharge circuit according to claim 13. Rampold does not disclose a relay connected between the power source and a drain of the first transistor. Ninh teaches a precharge circuit wherein the relay is configured to bypass the first transistor when a predetermined voltage threshold has been exceeded. It would have been obvious to one of ordinary skill in the art at the time of the invention to place a relay in parallel to the precharge circuit. The reason for doing so is to carry the heavy load currents after the capacitor is charged.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Cole (US 6,335,654) and Conners (US 5,283,707) disclose similar inrush circuits. Ball (US 7,099,135) and Mercier (US 7,072,159) disclose thermal sensing inrush circuits. Malik (US 6,445,165) discloses the use of relays.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Harry Behm whose telephone number is 571-272-8929. The examiner can normally be reached on Business EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Karl Easthom can be reached on 571-2721989. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KARL EASTHOM
SUPERVISORY PATENT EXAMINER